

providing a first integrated circuit chip having a terminal and a signal terminal;

forming an electrically conductive connection between the terminal and the signal terminal of the first integrated circuit chip;

providing a protective structure that becomes conductive to dissipate electrostatic discharges;

providing a second integrated circuit chip having a terminal that is coupled to the protective structure;

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disposing the first integrated circuit chip and the second integrated circuit chip adjacent one another;

electrically connecting the signal terminal of the first integrated circuit to the terminal of the second integrated circuit chip;

connecting the terminal of the first integrated circuit chip to a terminal of a package; and

subsequent to connecting the terminal of the first integrated circuit chip to the terminal of the package, severing the electrically conductive connection between the terminal and

the signal terminal of the first integrated circuit chip using an energy pulse.

Claim 2 (amended). The method according to claim 1, wherein the severing step is performed by applying an electrical current pulse to the terminal of the second integrated circuit chip.

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Claim 3 (amended). The method according to claim 1, wherein the forming step includes:

forming the electrically conductive connection with a portion of reduced cross sectional area as compared to the rest of the connection; and

dimensioning the portion to dissipate electrostatic discharges between the terminal and the signal terminal of the first integrated circuit chip and to be severed during application of the energy pulse in the severing step.

Claim 4 (amended). The method according to claim 3, wherein the energy pulse used in the severing step is an electrical current pulse applied to the terminal of the second integrated circuit chip.

Claim 5 (amended). The method according to claim 1,
including:

disposing the first integrated circuit chip and the second
integrated circuit chip in a package having terminal pins so
that the signal terminal of the first integrated circuit chip
is not accessible from outside of the package; and

connecting the terminal of the first integrated circuit chip
and the terminal of the second integrated circuit chip to a
respective terminal pin of the package.

Claim 7 (amended). The method according to claim 1, wherein
the disposing step is performed so that terminal of the second
integrated circuit chip is not covered by the first integrated
circuit chip.

Claim 8 (three-times amended). A method for producing an
electrical connection between integrated circuit chips, which
comprises:

providing a first integrated circuit chip having a surface;

disposing first and second terminal pads on the surface of the
first integrated circuit chip;

forming an electrically conductive connection between the first and second terminal pads of the first integrated circuit chip;

providing a second integrated circuit chip having a surface;

disposing first and second terminal pads on the surface of the second integrated circuit chip;

providing a protective structure acting as a switch that becomes conductive when there is an overvoltage to dissipate an electrostatic discharge to a line for a supply voltage;

electrically coupling at least the first terminal pad of the second integrated circuit chip to the protective structure;

disposing the surfaces of the first integrated circuit chip and the second integrated circuit chip longitudinally adjacent one another so that the first and second terminal pads of the second integrated circuit chip are not covered by the first integrated circuit chip;

electrically joining at least one of the first and second terminal pads of the first integrated circuit chip to one of the first and second terminal pads of the second integrated circuit chip;

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severing the electrically conductive connection using an energy pulse.

D3

Claim 11 (amended). The method according to claim 8, including electrically joining the other one of the first and second terminal pads of the first integrated circuit chip to the other one of the first and second terminal pads of the second integrated circuit chip.

D4

Claim 18 (amended). The method according to claim 1, which comprises performing the severing step before packaging the first integrated circuit chip and the second integrated circuit chip.